Study of Self-Heating Effects in GaN HEMTs

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***Abstract* — Pulsed RF and IV characterizations are performed on power GaN HEMTs. These measurements are carried out at different temperatures for the first time to understand self-heating effects and to investigate the possibility of improving heat dissipation mechanisms. These measurements are the basis for robust large-signal models.**

I. Introduction

The wireless communication market is growing rapidly and there is a great demand for high power transistors for applications such as phased array antennas and base stations. In these days, available power transistors are in the 1W/mm range. Candidates to fill the need for higher output power are Si-LDMOS, SiC and GaN based transistors. They offer power densities in the few W/mm range because of their high breakdown voltage [1-7]. GaN compared to SiC and Si-LDMOS, offers higher cut off frequencies and maximum frequencies of oscillation ($f_T \approx$ 25 GHz, and $f_{MAX} \approx$ 33 GHz) [2,4,5].

Studying devices under pulsed conditions and for different temperature of operation allows one to understand the thermal behavior and answer the question of whether or not improvements in heat sinks will ameliorate the device's characteristic. Additionally, studying devices under these condition enables one to build more robust large-signal models that help understand the device physics [6,8,9,10].

In this work we present fully characterized GaN HEMTs under pulsed conditions with the temperature as an additional parameter. Both IV and power RF characteristics are achieved in a continuous and pulsed mode up to 25 GHz and at temperatures down to 65 K.

II. Experimental Setup

The experimental setup consists of two pulse bias generators, a frequency source synchronized with the pulse generator enabling a pulse RF signal that is amplified to attain the required input power level at the DUT. The current is monitored with a digitizing scope through a current probe. The RF power is monitored with a peak power meter. Measurements are achieved at a gate baseline that is in the pinch-off region of the DUT. Both the drain and RF pulse width are shorter and delayed by few 100ns in order to center them in the gate pulse. Fig. 1 presents a diagram of the setup used.

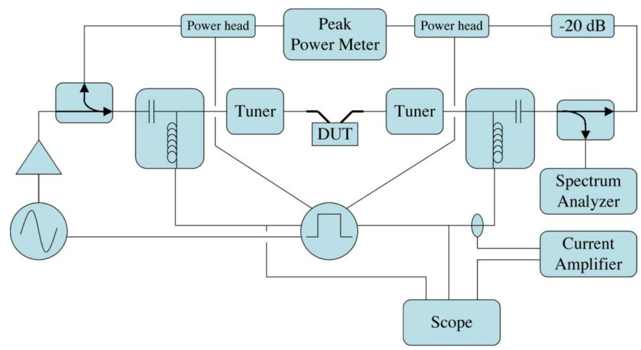

Fig. 1 Schematic of the measurement system.

Measurements have been carried out on AlGaN/GaN HEMTs from 300K to 65 K using a cryogenic probe station [4,9]. The samples are provided by CREE Inc. and are grown on a SiC substrate, with a gate width of 125 µm per finger. Measurements were performed on different devices with various gate lengths and number of fingers. In this work we present the results of a 2-finger device with a gate length L_G = 0.35 µm, a gate to source L_{GS} = 0.1 µm, and gate to drain L_{GD} = 3 µm.

III. Influence On Large Signal Modeling

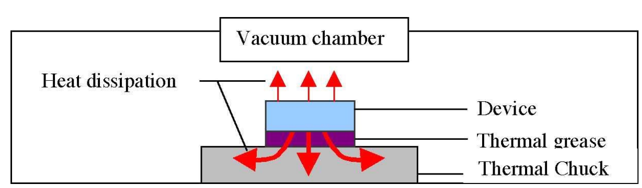

Fig. 2. Heat dissipation and thermal path for measurements.

The discrete device is mounted in a high vacuum cryogenic chamber cooled by a closed cycle helium refrigerator, as shown in Fig. 2. To insure good heat dissipation from the device to the cold head a perfect contact needs to be guaranteed. This is achieved with a thermal grease compound. Studying devices under these conditions allow us to understand the transistor's junction temperature under pulsed and continuous mode of operation and enable us to accurately build a robust model that include those parameters. In Fig. 3 we show the large-signal model extraction procedures [6].

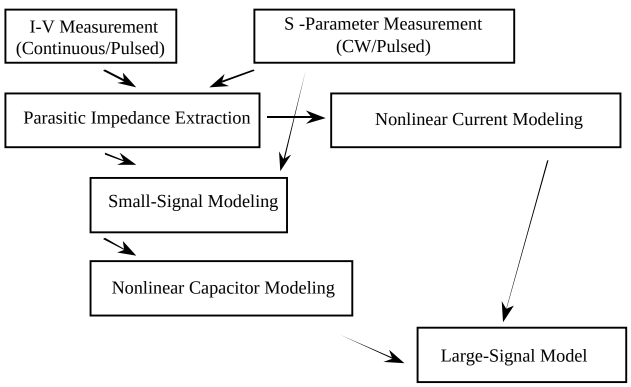

Fig. 3. Large-signal modeling flow diagram.

IV. RESULTS

The GaN HEMT DC characteristics show an increase in the drain current and the device transconductance while operating at reduced temperature (Fig. 4). The improvements are results of an increase in electron mobility [12].

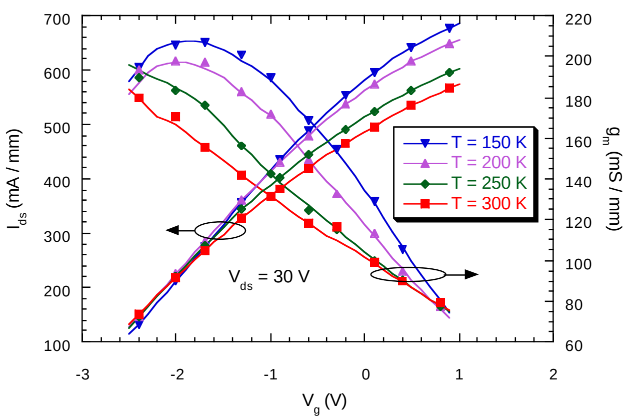

Fig. 4 Transconductance and drain current versus V_{GS} for various temperatures at V_{DS} = 30 V.

Fig. 5 exhibits pulsed-IV measurement characteristics at 300 K for various duty-cycle at 0 V gate bias and a pulse period of 100 µs. By gradually reducing the pulse width the negative slope of the $I_{DS}(V_{DS})$ characteristics becomes less important.

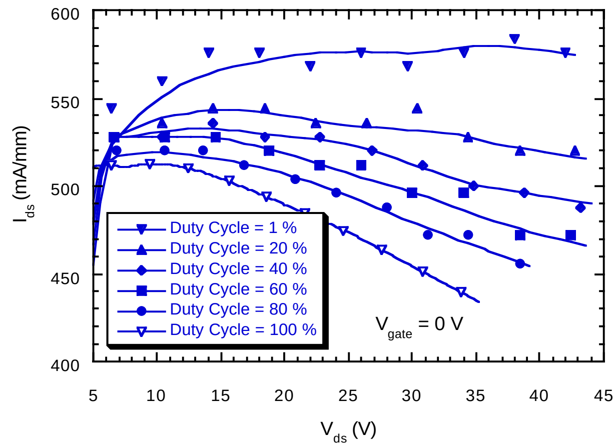

Fig. 5. Drain current for various duty cycles at V_{GS} = 0 V, at 300 K.

Fig. 6 compares the drain-to-source current at 300K and 65K under pulsed and continuous mode of operation. Pulsed characteristics are obtained with a signal period of 100 µs, and a pulse width of 1 µs on the drain side. Unlike at 300 K, pulsed and continuous I-V characteristics at T = 65 K correlate for drain voltages larger than 15 V. The mismatch observed at 65 K at low drain voltages has been reported in [13].

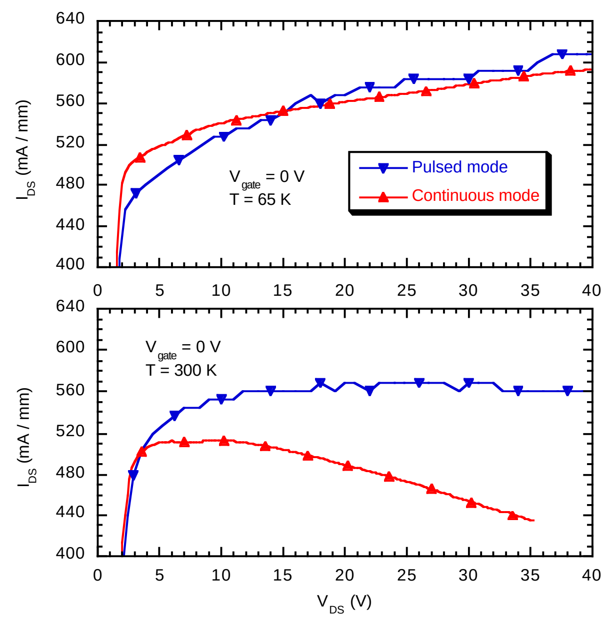

Fig. 6. Drain current at V_{GS} = 0 V under pulsed and continuous conditions at T = 65 K and T = 300 K.

Fig. 7 shows the temperature effects on DC-$I_{DS}(V_{DS})$ and DC-$I_{GS}(V_{DS})$ characteristics. At any temperature, it is possible to define the drain voltage threshold as the drain voltage value at which the drain current starts to decrease. It is noteworthy that as the temperature decreases, the drain voltage threshold increases. This is interpreted as an extension of the drain voltage range for which the DUT does not suffer from self-heating. At the same time a decrease in the temperature reduces the gate current.

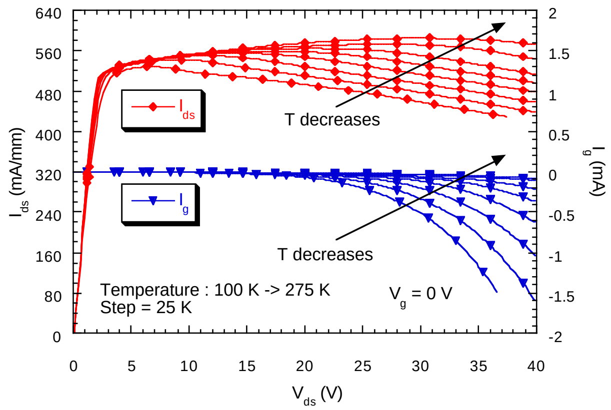

Fig. 7. Drain and gate current for various temperatures at V_{GS} = 0 V.

At any bias and temperature conditions it is possible to define the pulse width threshold as the pulse width that leads to a drain current saturation. Fig. 8 displays the pulse width threshold for V_{DS} = 45 V, V_{GS} = 0 V, a period of 100 µs, and at several temperatures. We observe that at 150 K, the drain current is saturated at all available pulse widths. This is perceived as an absence of any heating effects. Above 225 K the drain current could not be saturated at any available duty-cycle (the minimum duty-cycle used was 1 %). Therefore, it is possible to say that the pulse width threshold is below 1 µs for temperatures greater than 225 K. For temperatures between 150 K and 225 K saturation of the drain current was observed, and thus a threshold value was extracted. We observed that the threshold value to achieve drain current saturation increases while temperature decreases, meaning that a reduction in the external temperature decreases self-heating effects in the device. Fig. 8 also shows the pulse width threshold as a function of temperature for two different bias conditions.

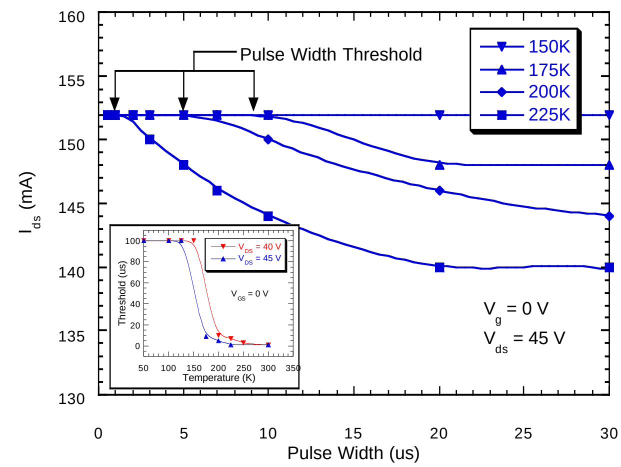

Fig. 8. Drain current versus pulse width for pulse width threshold determination (isothermal environment) at various temperatures.

Fig. 9 shows the short-circuit current gain and the maximum available gain under different temperature conditions. The cutoff frequency (f_T) and the maximum frequency of oscillation (f_{MAX}) improve while reducing the temperature of operation.

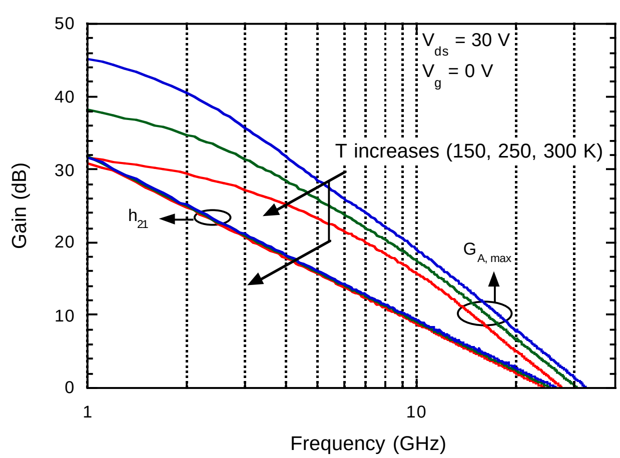

Fig. 9. Short circuit current gain and maximum available gain at different temperatures (300, 250, 150 K)

Finally, Fig. 10 shows the RF power performance of the GaN HEMT sample when operated at reduced lattice temperature. Measurements are achieved under pulsed and CW mode of operation. As the temperature decreases the heating effects become less important resulting in little difference between CW and pulsed RF/bias power measurements. The pulsed power measurements are achieved with a 5µs pulse width on the gate side, a 3µs pulse width for the drain, and a 2µs pulse width for the RF signal.

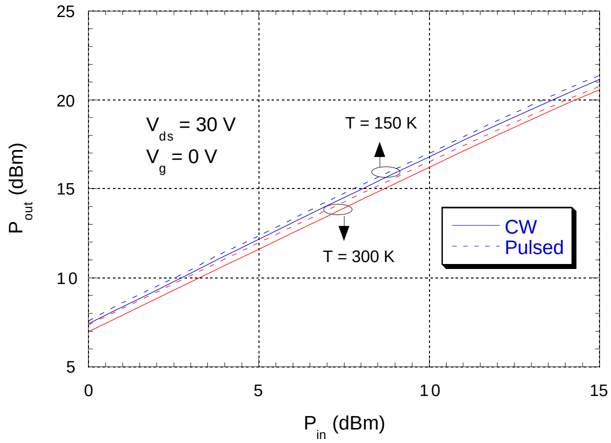

Fig. 10. Output power versus frequency under pulsed and continuous conditions into 50 Ohms termination at T = 150 K and T = 300 K (V_{DS} = 30 V, V_{GS} = 0 V).

V. Conclusion

Pulsed RF and I-V measurements are attained for the first time on GaN HEMT samples at different temperature conditions. The measurement results give an in depth understanding of the device behavior and are the basis for robust large-signal device modeling. Additionally, these measurements allow the understanding of the self-heating effects in GaN-based transistors and the possibility for device structure improvement resulting in better device performance.

Acknowledgement

The authors wish to acknowledge their sponsor John Zopler from the Office of Naval Research, CREE Inc. for providing the devices, and J. Mulligan and W. Pribble from CREE Inc. for all their support.

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